2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5518BP-20, TC5518BPL-20
TC5518BD-20, TC5518BDL-20
TC5518BF-20, TC5518BFL-20

DESCRIPTION

The TC5518BP/BD/BF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5518BP/BD/BF has two chip enable inputs, $\overline{CE}_1$ and $\overline{CE}_2$, which are used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5518BP/BD/BF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518BPL/ BDL/BFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature available.

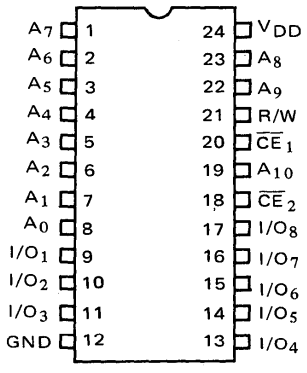
And the TC5518BP/BD/BF is pin compatible with 2716 type EPROM. This means that the TC5518BP/ BD/BF and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current
  0.2μA (Max.) at Ta = 25°C } TC5518BPL/
  1.0μA (Max.) at Ta = 60°C } BDL/BFL-20
  1.0μA (Max.) at Ta = 25°C } TC5518BP/BD/
  5.0μA (Max.) at Ta = 60°C } BF-20
- Single 5V Power Supply: 5V±10%
- Data Retention Supply Voltage
  2.0 ~ 5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC} = 200ns (Max.)
- Two Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$) for Simple Memory Expansion and Battery Back Up
- On-chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC5518BP/BPL
  Cerdip DIP : TC5518BD/BDL
  Platic FP : TC5518BF/BFL

PIN CONNECTION

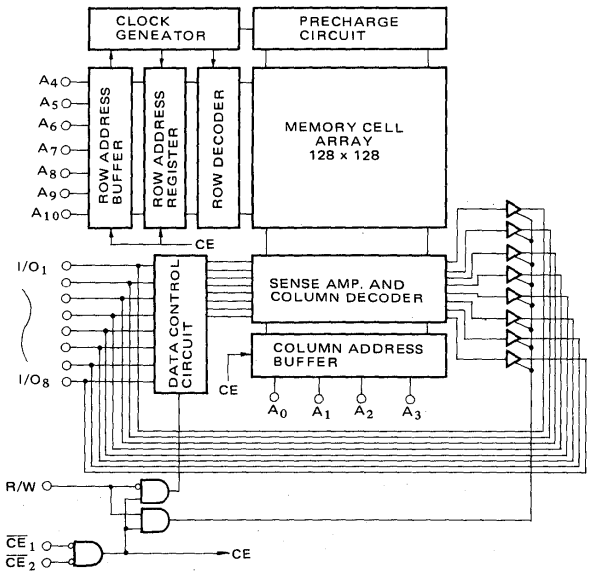
(Top VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}_2$	$\overline{CE}_1$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim _8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	L	L	Stable	Data In	I_{DDO}
** Standby 1	*	H	*	*	High Impedance	I_{DDS}
** Standby 2	H	*	*	*	High Impedance	I_{DDS}

Note; *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD}+0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

*: Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{DH}	Data Retention Voltage	2.0	−	5.5	V

D.C. CHARACTERISTICS (Ta = −30°C ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			−	−	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}_2 = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			−	−	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	−	mA
I_{DDS1}	Standby Current	$\overline{CE}_2$ = 2.2V or $\overline{CE}_1$ = 2.2V			−	1.0	3.0	mA
I_{DDS2}		$\overline{CE}_2 \geqq V_{DD}$ −0.5V or $\overline{CE}_1 \leqq V_{DD}$ −0.5V, V_{DD} = 2 ~ 5.5V	TC5518BPL /BDL/BFL-20	Ta=25°C	−	−	0.2	mA
				Ta=60°C	−	−	1.0	μA
			TC5518BP/ BD/BF-20	Ta=25°C	−	0.05	1.0	
				Ta=60°C	−	−	5.0	
				Ta=85°C	−	−	30	
I_{DDO1}	Operating Current	t_{cycle} = 200ns, $\overline{CE}_1$ = $\overline{CE}_2$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		−	−	30	mA
I_{DDO2}			$V_{IN} = V_{DD}$/GND		−	−	25	
I_{DDO3}		t_{cycle} = 1μs, $\overline{CE}_1$ = $\overline{CE}_2$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		−	−	10	
I_{DDO4}			$V_{IN} = V_{DD}$/GND		−	−	5	

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	−	5	10	pF
$C_{I/O}$	Input/Output Capacitance	−	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = –30 ~ 85°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	–	–	ns
t_{ACC}	Access Time	–	–	200	ns
t_{CO1}	$\overline{CE}_1$ to Output Valid	–	–	200	ns
t_{CO2}	$\overline{CE}_2$ to Output Valid	–	–	200	ns
t_{COE}	$\overline{CE}_1$ or $\overline{CE}_2$ to Output Active	10	–	–	ns
t_{OD}	Output High-Z from Deselection	–	–	60	ns
t_{OH}	Output Hold from Address Change	20	–	–	ns

Write Cycle

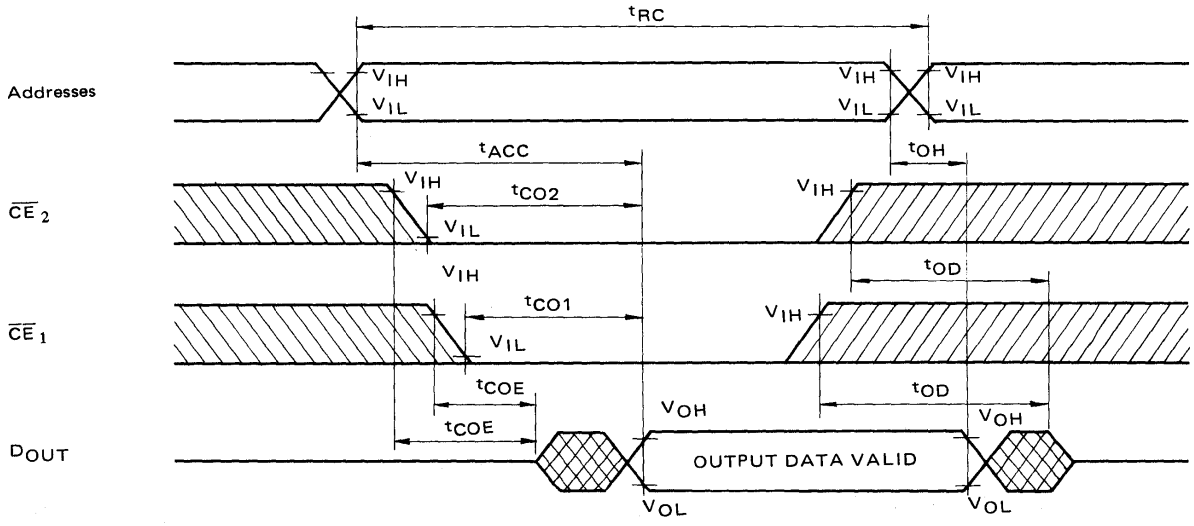
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	–	–	ns
t_{WP}	Write Pulse Width	150	–	–	ns
t_{AW}	Address Set up Time	0	–	–	ns
t_{WR}	Write Recover Time	0	–	–	ns
t_{ODW}	Output High-Z from R/W	–	–	60	ns
t_{OEW}	Output Active from R/W	10	–	–	ns
t_{DS}	Data Set up Time	90	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns

A.C. TEST CONDITIONS

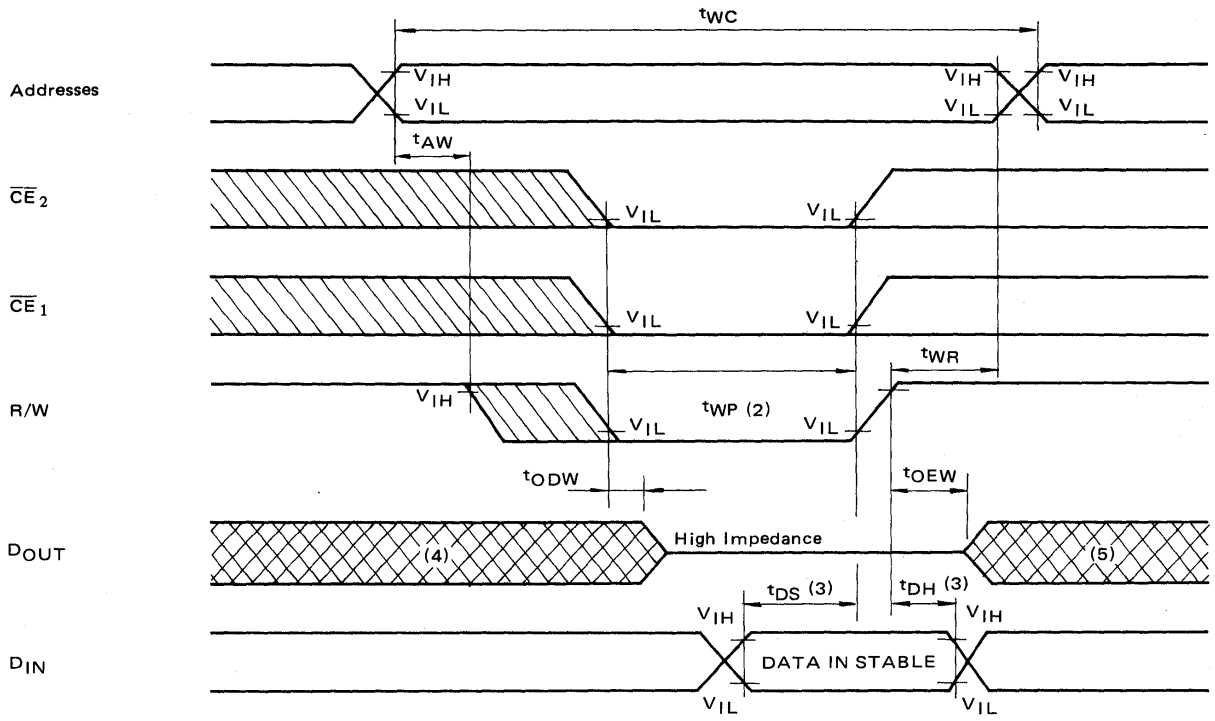
Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Mesurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

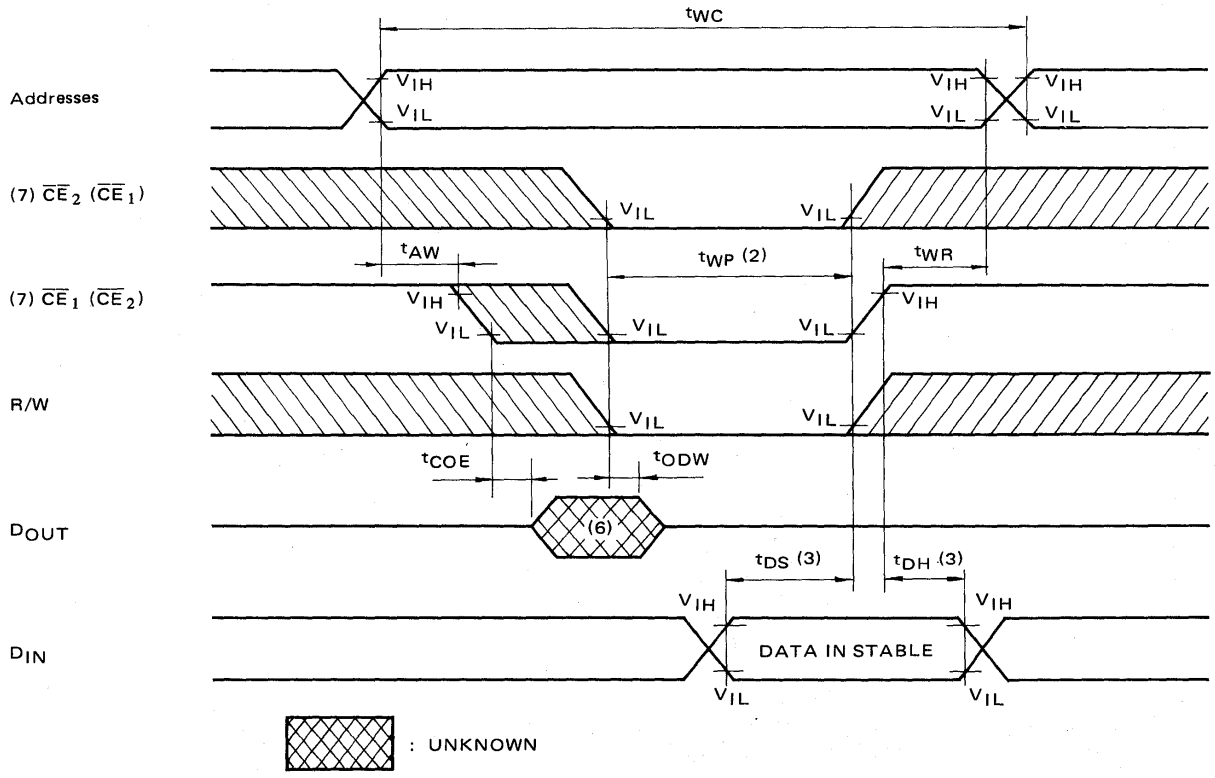
Read Cycle (1)



Write Cycle 1.



Write Cycle 2.

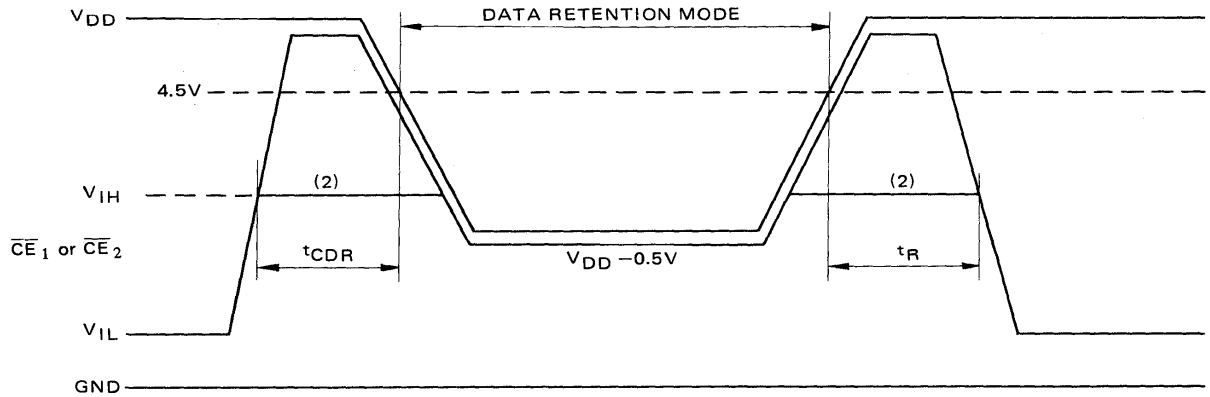


Note: (1) R/W is high for a Read Cycle.
(2) t_{WP} is specified as the logical "AND" or $\overline{CE}1$, $\overline{CE}2$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}1$, $\overline{CE}2$ or R/W going low to the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.
(3) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.
(4) If the $\overline{CE}1$, or $\overline{CE}2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(5) If the $\overline{CE}1$ or $\overline{CE}2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}1$ or $\overline{CE}2$ low transition, the output buffers remain in a high impedance state in this period.
(7) A write occurs during the overlap of a low $\overline{CE}1$, low $\overline{CE}2$ and low R/W.
In write cycle 2, write is controlled by either $\overline{CE}1$ or $\overline{CE}2$.

DATA RETENSION CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5518BPL/ BDL/BFL-20	Ta = 25°C	–	–	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5518BP/ BD/BF-20	Ta = 25°C	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recover Time			t_{RC}(1)	–	–	μs

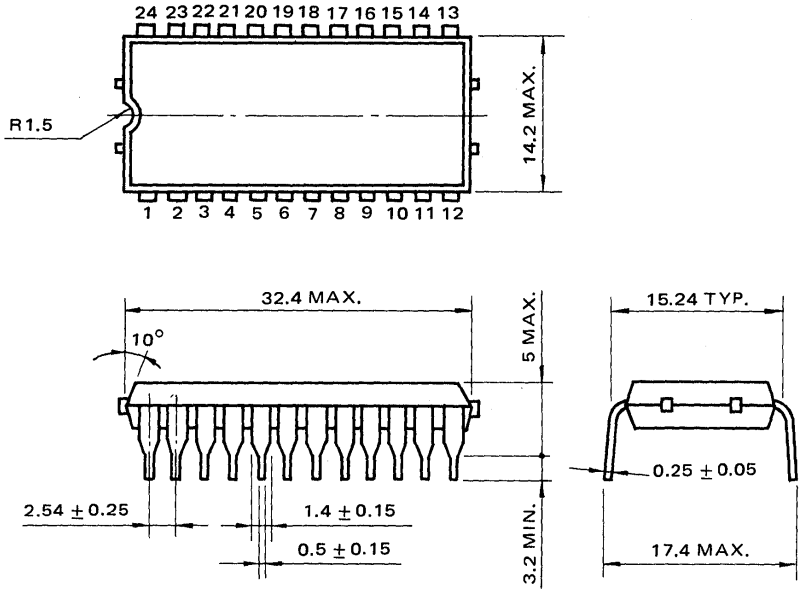
Note (1) t_{RC} : Read Cycle Time



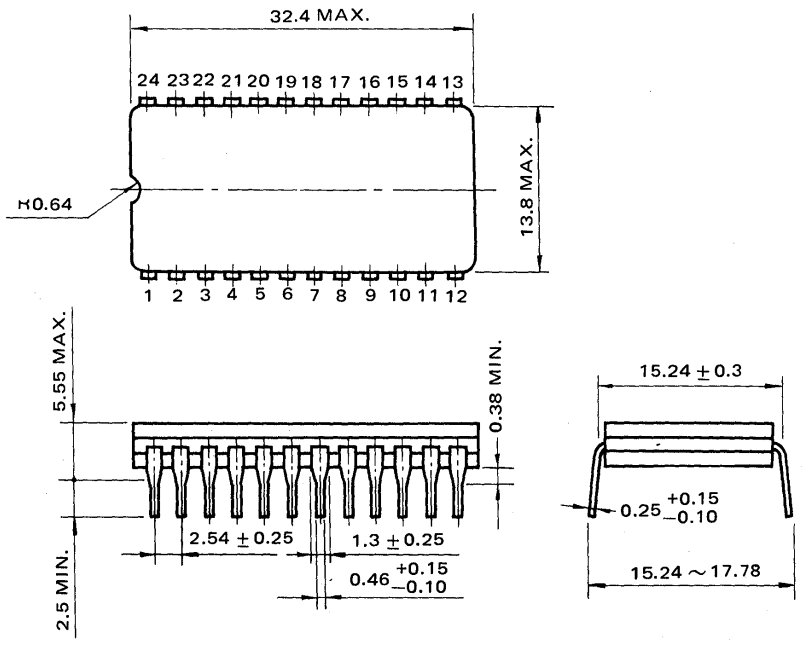
Note (2) if the V_{IH} level of $\overline{CE}_2$ ($\overline{CE}_1$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

OUTLINE DRAWINGS

- **Plastic DIP**

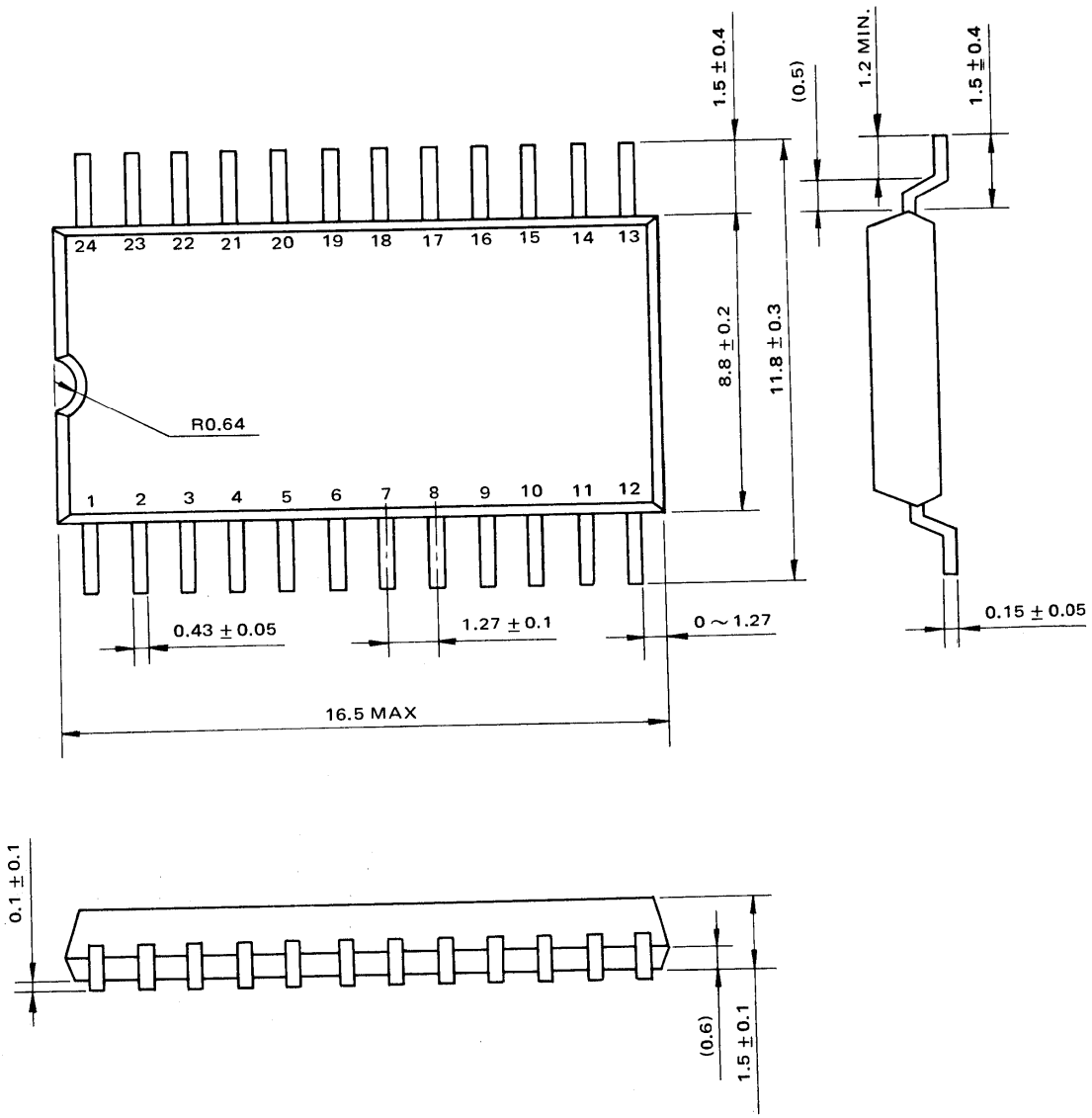


- **Cerdip DIP**



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudianl position with respect to No. 1 and No.24 leads.
All dimensions are in millimeters.

- **Plastic FP**



Note: Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

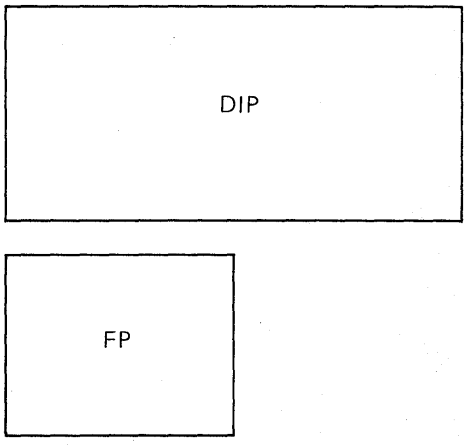
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

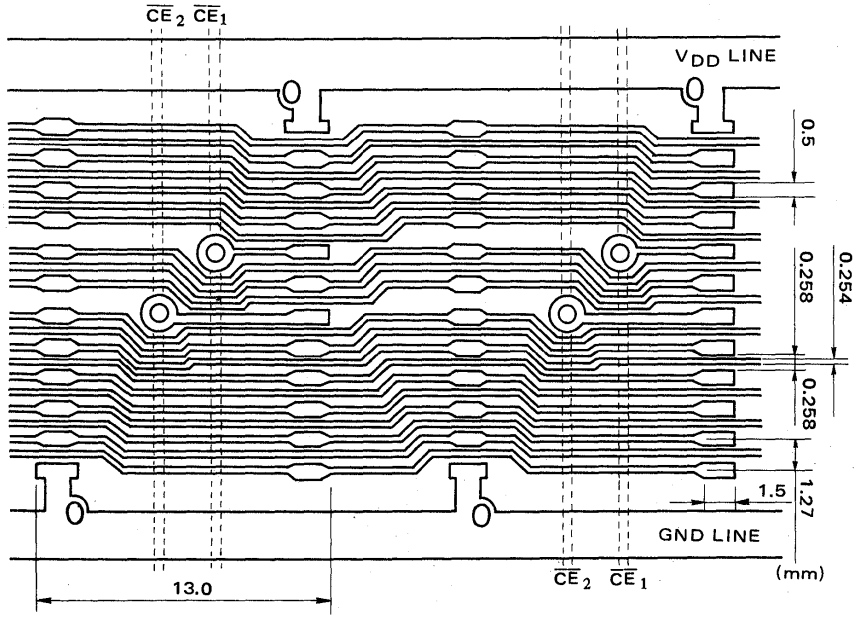
2. Comparison in occupied space



3. Advantage of this package

Small dimensions
Capability of High Density Assembly
Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

Distributed by